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**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF OREGON
PORTLAND DIVISION**

MEMORY INTEGRITY, LLC,

Case No.: 3:15-cv-00262-SI

Plaintiff,

Defendant Intel Corporation's
REPLY BRIEF IN SUPPORT OF ITS
MOTION TO LIMIT THE NUMBER OF
ASSERTED CLAIMS

v.

INTEL CORPORATION,

ORAL ARGUMENT REQUESTED

Defendant.

INTEL'S REPLY BRIEF IN SUPPORT OF ITS MOTION TO LIMIT THE NUMBER OF
ASSERTED CLAIMS

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I. INTRODUCTION

MI concedes that it “cannot present a trial on 118 claims” and that it intends to ultimately reduce the number of claims to no more than 25. (Dkt. 128 [MI’s Opp’n Br.] at 14-15.) Setting aside that 25 claims is still far too many to present at trial, MI’s opposition brief confirms that the primary dispute is not *whether* MI should be required to reduce the number of asserted claims, but instead *when* it should be required to do so. The only remaining question is how much longer the parties and the Court should be required to expend resources litigating *the at least 93 claims* that MI admits it will eventually drop. MI should not be permitted to force Intel to continue litigating an unreasonably large number of claims only to cherry pick on the eve of trial the small number of claims it will actually assert. Each of MI’s arguments to the contrary fails.

II. ARGUMENT

A. Intel Is Not Required to Show that the Asserted Claims Raise Duplicative Issues of Infringement and Invalidity.

MI first argues—citing to the Federal Circuit’s holding in *In re Katz Interactive Call Processing Patent Litigation*, 639 F.3d 1303 (Fed. Cir. 2011)—that Intel’s motion should be denied because it purportedly has not shown that the asserted claims are duplicative. (MI’s Opp’n Br. 8-10.) MI is wrong.

First, contrary to MI’s assertions, *Katz* explicitly rejected the argument that the *moving defendant* is required to show duplication among claims. Specifically, the Federal Circuit rejected the plaintiff’s argument that the district court “should have required the appellees [i.e., defendants] to bear the burden to show that issues were duplicative.” *Katz*, 639 F.3d at 1311. The court instead held that “it would be more efficient to require [plaintiff] *Katz* to point out those unselected claims that raised separate issues of infringement and invalidity.” *Id.* at 1312;

see also Stamps.com Inc. v. Endicia, Inc., 437 F. App'x 897, 902-03 (Fed. Cir. 2011) (summarizing *Katz* and making no reference to defendant's alleged requirement to show duplication).

Although the court noted that the defendants in *Katz* “made a convincing showing that many of the claims are duplicative” (MI's Opp'n Br. 8 (quoting *Katz*, 639 F.3d at 1311)), the court did **not** hold that such a showing is necessary. Instead, the court held that the “production burden” of showing that the claims raise unique issues of validity and infringement should presumptively be “allocate[d]” to the **plaintiff**, not the defendant. *See Katz*, 639 F.3d at 1311 (“When the claimant is in the best position to narrow the dispute, allocating the production burden to the claimant will benefit the decisionmaking process and therefore will not offend due process unless the burden allocation unfairly prejudices the claimant's opportunity to present its claim.”). *Katz* thus stands for precisely the opposite of the proposition for which MI cites it.

MI's misreading of *Katz* has been consistently rejected by courts in this Circuit and elsewhere. *See Thought, Inc. v. Oracle Corp.*, 2013 WL 5587559, at *2 (N.D. Cal. Oct. 10, 2013) (“[T]he Court does not agree that *In re Katz* requires defendants to make a prima facie showing of duplication in order to require a reduction in the number of asserted claims from a demonstrably unmanageable amount, here 102, to a manageable one.”); *Masimo Corp. v. Philips Elecs. N. Am. Corp.*, 918 F. Supp. 2d 277, 283 (D. Del. 2013) (“Masimo suggests the only legal standard recognized by the Federal Circuit in *In re Katz* was the duplicativeness of the claims. That assumption is not accurate.”).¹

¹ MI's reliance on *Automated Merchandising Systems, Inc. v. Crane Co.*, No. 3:03-cv-00088, Dkt. 548 (N.D.W. Va. Feb. 15, 2012), and *Avocent Redmond Corp. v. Rose Electronics*, 2012 WL 4903270 (W.D. Wash. May 29, 2012), for the proposition that defendants are required to show duplication under *Katz* (*see* MI's Opp'n Br. 9-10), is misplaced. Respectfully, those cases incorrectly interpret *Katz*'s holding. In any event, both cases are distinguishable on the

Second, there is significant duplication among the asserted claims. As MI concedes, “all five patents relate to cache coherency in microprocessors.” (MI’s Opp’n Br. 10.) Specifically, each is directed to maintaining cache coherence in the context of the same overall type of computer system—a “multiple cluster, multiple processor system” in which processors within a cluster are connected in a “point-to-point architecture.” (’409 patent at 1:22-26, 2:21-50, 4:31-35, 6:8-14, 6:36-42; ’636 patent at 1:40-45, 2:40-3:1, 5:7-11, 7:5-11, 7:33-40; ’121 patent at 2:19-48, 4:36-40, 6:10-16, 6:38-44; ’206 patent at 3:9-15, 3:36-42; ’254 patent at 3:12-18, 3:39-45.)

The patents share common inventors and have overlapping specifications (including many common figures). The ’636 patent, for example, states that it is “related to” the application that issued as the ’409 patent, and its specification significantly overlaps with that of the ’409 patent. (’636 patent at Cover Page, 1:7-9, Figs. 1A-7.) The ’121 and ’206 patent specifications similarly overlap with the ’409 and ’636 patents. (’121 patent at Cover Page, Figs. 1A-6; ’206 patent at Cover Page, 1:6-10, Figs. 1A-3.) The ’254 patent is a continuation of the ’206 patent and thus shares a specification with that patent. (’254 patent at Cover Page.) Moreover, many of

facts. In *Automated Merchandising*, the plaintiff had ***already reduced the number of claims*** from 116 to 26 in response to defendant’s motion. The court noted that the defendant had failed to show that 26 claims asserted in four consolidated actions “is not manageable.” *Automated Merchandising*, No. 3:04-cv-00080, at 4-5. Here, Intel has shown why 118 claims is not manageable in this single case. Further, in both *Avocent* and *Automated Merchandising*, the defendants “failed to make even a *prima facie* showing that plaintiff[s] ha[d] asserted superfluous claims.” *Avocent*, 2012 WL 4903270, at *1; *Automated Merchandising*, No. 3:03-cv-00088, Dkt. 548, at 4 (noting that, in contrast to *Katz*, “there has been no showing” that “many of the claims are duplicative”). Intel, by contrast, has demonstrated the similarities among the asserted claims and the technologies disclosed in the patents-in-suit.

the asserted claims share common elements, including, for example, (1) multiprocessor systems,² (2) point-to-point architectures,³ (3) cache coherence controllers,⁴ and (4) speculative probing.⁵

The close relationship among the patents and the similarity of many of the claimed features are more than sufficient to establish duplication among the 118 asserted claims. *Havco Wood Prods., LLC v. Indus. Hardwood Prods., Inc.*, 2011 WL 5513214, at *6 (W.D. Wis. Nov. 10, 2011) (holding that reduction to 15 claims is proper where “the patents are all related and the claims significantly overlap”); *Thought*, 2013 WL 5587559, at *2 (noting that courts should “look to whether the patents at issue have common genealogy” when determining whether to impose limitations on the number of asserted claims (citing *Katz*, 639 F.3d at 1311)).

Third, MI’s assertion that Intel purportedly has not shown duplication misses the point. Specifically, MI argues (relying on its misreading of *Katz*) that Intel has not established that the number of claims should be reduced (*see* MI’s Opp’n Br. 9-10), yet MI ***has already conceded*** that the number of asserted claims should (and will) be reduced (*id.* at 14-15). *See Masimo*, 918 F. Supp. 2d at 284 (“Masimo argues . . . that each claim is a distinct invention with unique features, which suggests no claim reduction could ever occur in any matter. . . . Masimo’s underlying gripe is timing—being required to reduce its claims at the present stage, and not that the number of claims asserted would eventually be reduced.”). Thus, the only issues in dispute

² (*See, e.g.*, ’636 patent at claims 11-14; ’409 patent at claims 25-30, 51-52.)

³ (*See, e.g.*, ’636 patent at claims 15-18, 21, 25-26, 34; ’409 patent at claims 1-3, 6-12, 18-20, 22-23, 25-30, 42-43, 45-49, 51-52; ’121 patent at claims 1-6, 8, 11-17, 19-25; ’206 patent at claims 1-4, 7, 12, 14-15, 19-22, 24-29, 31-32; ’254 patent at claims 2-3, 5-7.)

⁴ (*See, e.g.*, ’636 patent at claims 11-18, 21-31, 33-35; ’409 patent at claims 1-3, 6-12, 18-20, 22-23, 25-30, 51-52; ’121 patent at 3, 5-6; ’206 patent at claims 1-4, 7, 12, 14-15, 19-22, 24-32, 34-44 (“interconnection controller,” which is same as “cache coherence controller”); ’254 patent at claims 1-8 (same).)

⁵ (*See, e.g.*, ’636 patent at claims 22-31, 33-35; ’409 patent at claims 7-12, 18-20, 22-23, 25-30, 42-43, 45-49.)

are when and the extent to which MI should reduce the number of asserted claims. As demonstrated in Intel’s opening brief, “[t]he time for identifying critical issues and for narrowing the scope of this litigation, if not passed, is now” (Dkt. 115 [Intel’s Br.] at 14 (quoting *High Point Sarl v. Sprint Nextel Corp.*, 2010 WL 9497168, at *2-3 (D. Kan. Aug. 18, 2010))) and the number of asserted claims should be reduced to 15 (*id.* at 13, 15-16 (quoting *Network Protection Scis., LLC v. Fortinet, Inc.*, 2013 WL 1949051, at *2 (N.D. Cal. May 9, 2013) (noting that even 15 claims “is still too large to be tried”)))).

B. A Reduction in the Number of Asserted Claims Is Not Premature in Light of the Year’s Worth of Discovery that Has Already Occurred in this Case.

MI next argues that Intel’s motion is premature and that, given the state of discovery, MI “does not have sufficient information at this time to make an informed decision in reducing the number of asserted claims.” (MI’s Opp’n Br. 13.) Specifically, MI argues that “Intel has not provided a meaningful response to MI’s interrogatory seeking Intel’s non-infringement contentions,” and that MI cannot reduce its claims until it receives that response. (*Id.* at 12.) MI is again wrong.

First, the premise of MI’s argument—that discovery must be completed or substantially completed before a reduction in claims is appropriate—is incorrect and has been rejected by most courts that have addressed this issue. As explained in Intel’s opening brief, “[t]he vast majority of courts that have ordered claim reduction have done so prior to claim construction” and the completion of discovery. (Intel’s Br. 13-14 (quoting *Arctic Cat, Inc. v. Polaris Indus. Inc.*, 2015 WL 3756409, at *4 (D. Minn. June 12, 2015)).) ***MI does not even attempt to distinguish these cases.*** Instead, MI relies on only a few district court decisions that have reached contrary conclusions based on facts that are plainly distinguishable from those presented here. (*See* MI’s Opp’n Br. 12.) MI’s reliance on these opinions is misplaced.

In *DataQuil Ltd. v. High Tech Computer Corp.*, No. 3:08-cv-00543, Dkt. 87 (S.D. Cal. Mar. 16, 2011), for example, the parties “agree[d] that the number of patent claims does not bear on the parties’ ability to take discovery from deposition witnesses.” *Id.* at 2. In light of that agreement, the court found that the defendant had not shown that the case was “unwieldy or will become unwieldy before the conclusion of discovery.” *Id.* Here, by contrast, Intel has shown precisely why the large number of currently asserted claims would unduly burden Intel’s ability to take and defend the depositions of both experts and key fact witnesses. The *Realtime Data, LLC v. Packeteer, Inc.*, 2009 U.S. Dist. LEXIS 131805 (E.D. Tex. Mar. 16, 2009), decision, on which MI also relies, pre-dates the Federal Circuit’s *Katz* decision. In fact, the *Realtime Data* court noted in its decision that, at the time, “the Federal Circuit ha[d] not directly addressed the issues surrounding when and how a district court may limit the asserted claims in a patent case.” *Id.* at *21. *Katz* and the decisions that have followed plainly confirm the appropriateness of a reduction in claims prior to the close of discovery. *See Katz*, 639 F.3d at 1308-13.⁶

Second, discovery has been ongoing in this case for a full year and the deadline for the substantial completion of document production is less than three weeks away. (See Dkt. 87 [Scheduling Order] at 1). During discovery, “the parties have . . . exchanged infringement and invalidity contentions, preliminary claim constructions and core technical documents,” which—as the cases confirm—is more than sufficient for MI to determine which claims to assert. *Thought*, 2013 WL 5587559, at *3; *High Point*, 2010 WL 9497168, at *2-3 (ordering reduction

⁶ MI further complains that Intel did not propose deadlines for limiting the number of claims in its proposed case schedules early in the case. (See MI’s Opp’n Br. 1, 2, 11.) But these complaints demonstrate the inconsistency of MI’s positions. MI is effectively arguing that Intel should have sought a limitation on the number of asserted claims earlier, while simultaneously arguing that issuing a restriction now would be premature. *See Havco*, 2011 WL 5513214, at *5 (“Havco’s response appears inconsistent, arguing both that IHP should have sought a limitation earlier and that issuing a restriction now would be premature.”).

of asserted claims from 117 to 20 where discovery was ongoing, the parties had exchanged non-infringement contentions, and claim construction briefs were underway). If MI has failed to use the significant amount of information in its possession to conduct the necessary investigation to limit the number of claims, that is MI's fault, not Intel's.

Third, MI's characterization of Intel's discovery responses is incorrect and contradicted by the record. Intel has provided detailed contentions regarding its non-infringement position with respect to each asserted claim—a massive undertaking in light of the vast number of claims asserted and MI's failure to fully disclose its infringement theories in its contentions. In fact, in response to MI's requests, Intel provided a further forty-page explanation of its non-infringement positions on September 25. (Ex. 1 [Intel's Second Supp. Resp. to Interrog. No. 18].⁷) These responses—which contain far greater detail than MI itself has provided in discovery—give MI much more information than it needs or than the cases say is required to reduce the number of asserted claims. Indeed, many courts have ordered plaintiffs to reduce the number of asserted claims *before* the defendant disclosed its non-infringement positions, finding that plaintiffs should not be permitted to assert a large number of claims only to then cherry pick the ones it believes it can sustain. *See Medtronic Minimed Inc. v. Animas Corp.*, 2013 WL 3322248, at *2 (C.D. Cal. Apr. 5, 2013) (“Defendant will actually suffer greater prejudice if this Motion [to limit claims] is denied than Plaintiffs will suffer if the Motion is granted, for if Defendant has any hope of Plaintiffs voluntarily reducing the number of asserted claims, Defendant must first submit non-infringement and invalidity contentions . . . knowing full well that the vast majority of those contentions will become moot upon Plaintiffs’ reduction of claims shortly thereafter.”); *Oasis Research, LLC v. Adrive, LLC*, 2011 WL 7272473, at *2 (E.D. Tex. Sept. 13, 2011)

⁷ The exhibits to this reply brief are attached to the supporting Second Declaration of Arthur W. Coviello.

(ordering reduction in claims despite pending motion to compel defendant to respond to interrogatory).

At any rate, if MI believed that Intel's contentions were inadequate, it could have moved to compel (as noted by the case to which MI cites). *See Havco*, 2011 WL 5513214, at *6 (ordering reduction in claims and rejecting argument that defendant's allegedly "incomplete" discovery "responses or contentions" required that motion to limit the number of asserted claims be denied). But not only did MI never move to compel, it never even complained about any of Intel's discovery responses until *after* Intel requested that MI reduce the number of asserted claims. Having failed to raise any such concerns, MI cannot now reasonably complain that it lacks information necessary to reduce the number of asserted claims.⁸

C. MI's Continued Assertion of an Unreasonably Large Number of Claims Has, and Will Continue to, Prejudice Intel.

MI also argues—without citing to any support—that Intel is not prejudiced by MI's assertion of 118 claims, and that Intel's requested reduction would not significantly streamline discovery. (MI's Opp'n Br. 14.) These positions are contradicted by the facts, the law, and basic common sense.

First, Intel has been, and continues to be, prejudiced by the assertion of such a large number of claims. As explained in its opening brief, Intel was forced to prepare invalidity contentions addressing the multiple limitations of each of the more than one hundred asserted

⁸ MI's reliance on *Certusview Technologies, LLC v. S & N Locating Services, LLC*, No. 2:13-cv-00346, Dkt. 86 (E.D. Va. Mar. 19, 2014), is misplaced. (MI's Opp'n Br. 13.) In that case, the court denied defendants' motion to limit claims because a motion to compel defendants' responses to certain interrogatories regarding non-infringement and invalidity was pending. *See id.* at 5. The court went on to note that it "*fully expects* Plaintiff to" "reasonably limit the number of claims being asserted," and that it "has no intention of placing 68 claims before a jury." *Id.* Consistent with Intel's motion, the court subsequently limited plaintiff to 15 asserted claims. *See Certusview Techs., LLC v. S & N Locating Servs., LLC*, 2014 WL 4930803, at *5-6 (E.D. Va. Oct. 1, 2014).

claims under the many different potential infringement theories that MI could advance. This effort resulted in contentions totaling approximately 6,000 pages. That Intel “was able to” timely serve these contentions does not mean that doing so was not burdensome. (*See id.* at 13.) To the contrary, responding to MI’s infringement contentions for each of the then-asserted 110 claims was a massive undertaking. *See Network Protection*, 2013 WL 1949051, at *2 (referring to prior art search for only 50 claims as imposing “*a bone-crushing burden*” (emphasis added)). Because MI has already agreed that it would be appropriate to reduce the number of claims to no more than 25 before trial, Intel’s contentions for at least 85 of those claims will indisputably become unnecessary. *See Medtronic*, 2013 WL 3322248, at *2-3 (finding that requiring defendant to submit contentions addressing an unreasonably large number of claims “knowing full well that the vast majority of those contentions will become moot” is “unfair[ly] prejudic[ial]” to defendant).

Moreover, MI’s strategy of burying the handful of claims it ultimately will assert among a massive number of claims that it has no intention of asserting would keep Intel guessing right up to the eve of trial as to which claims and issues will actually be disputed. MI’s own cited cases confirm that MI should not be permitted to cherry pick claims in this manner. (*See* MI’s Opp’n Br. 9-10 (quoting *Avocent Redmond Corp. v. Rose Elecs.*, 2012 WL 4903270, at *2 (W.D. Wash. May 29, 2012) (noting that plaintiff’s litigation strategy of “assert[ing] an unreasonable number of claims” allowed it to “hid[e] the ball,” “apparently in the hopes that [its] opponent[] will be unable to identify or focus on the real issues in the case”); *id.* (“[B]y providing too much information and too many potential legal theories, [plaintiff is] disclosing nothing at all while driving the costs of this case into the stratosphere.”)); *see also* Intel’s Br. 16-17 (collecting additional cases).)

Indeed, MI's recent conduct with respect to claim construction briefing provides an example of the prejudice that Intel will continue to suffer if MI is not required to reduce the asserted claims now. After 8:00 pm Eastern, the night before the parties' opening claim construction briefs were due, MI dropped six claims thereby eliminating *five* disputed claim terms. (*See* Ex. 2 [2015-09-29 Email from Mr. Saunders to Mr. Coviello].)⁹ In light of the imminent briefing deadline, Intel already had expended considerable resources—including both time and briefing space—addressing the dropped terms when it could have been focused on terms and issues MI actually intended to pursue. After having forced Intel to unnecessarily devote substantial resources, MI apparently determined that it could not sustain its arguments and dropped the claims in which the terms appeared.¹⁰ MI should not be permitted to continue employing such tactics with respect to the case as whole.

Second, contrary to MI's assertions, a reduction in the number of claims would indisputably lessen discovery burdens. (*See* MI's Opp'n Br. 13-14.) A reduction would necessarily alleviate discovery burdens because "infringement and validity analyses must be performed on a claim-by-claim basis." *Amazon.com, Inc. v. Barnesandnoble.com, Inc.*, 239 F.3d 1343, 1351 (Fed. Cir. 2001). Thus, a reduction would, for example: allow Intel's experts to address only 15 instead of 118 claims; allow the parties to focus depositions—including of the

⁹ In light of MI's decision to drop these claims, the total number of asserted claims is now 112.

¹⁰ The three previously disputed claim terms were means-plus-function terms for which MI had been improperly attempting to eliminate the structures disclosed in the asserted patents. Several claims in the '636 and '409 patents, for instance, recite a "means for receiving" and "means for sending/forwarding" cache access requests and probes. (*See* '636 patent at claim 36; '409 patent at claims 34-38.) The patents expressly describe the structure required to carry out these receiving and sending/forwarding functions: a cache coherence controller having a coherent protocol interface "implemented . . . as a full crossbar or as separate receive and transmit units using . . . multiplexers and buffers." ('636 patent at 9:1-15; '409 patent at 8:4-18.) But MI's proposed construction improperly limited the corresponding structure to "a cache coherence controller [and] its coherent interface." (*See* Dkt. 125 [Joint Claim Chart] at 5-6.)

named inventors and key technical witnesses—on 15 instead of 118 claims; and allow the parties to focus their written discovery requests and responses—including discovery relating to invalidity, non-infringement, and Intel’s covenant not to sue defense—on 15 instead of 118 claims. MI’s argument that litigating 15 claims would not be more efficient than litigating nearly *eight times* that many claims defies the case law and common sense.

D. The Counterproposal MI Describes Was Never Presented to Intel and Is in any Event Unworkable and Prejudicial.

Finally, MI argues that, to the extent the Court requires MI to limit the number of asserted claims, the reduction should be “gradual” and staggered as the case proceeds (MI’s Opp’n Br. 15-16)—notwithstanding that this case has been pending for nearly two years. This is wrong.

As an initial matter, contrary to its representations, the counterproposal MI describes in its brief is not the counterproposal that it made to Intel. The counterproposal MI presented to Intel required the parties to *simultaneously* reduce their claims and prior art. (*See* Intel’s Br. 6-7; Dkt. 116 [First Coviello Decl.] ¶ 7; Dkt. 116-10, Ex. 10 [2015-08-26 Email from Mr. Coviello to Mr. Saunders].) Intel confirmed this understanding of MI’s proposal in correspondence, and MI never responded or disputed Intel’s understanding. (*See* Ex. Dkt. 116-10, Ex. 10 [2015-08-26 Email from Mr. Coviello to Mr. Saunders].) Yet MI now states that it “proposed that Intel reduce its asserted prior art references *after* each reduction by MI in the number of asserted claims.” (MI’s Opp’n Br. 16 n.2; Dkt. 129 [Saunders Decl.] ¶ 2 (emphasis added).) The first time this was communicated to Intel was in MI’s opposition brief.

In any event, MI’s new proposal is unworkable and does not address the concerns articulated in Intel’s opening brief. *First*, MI’s proposal still allows it to leave an unreasonably large number of claims in the case for far too long. Such a strategy would unfairly require Intel

to continue to expend massive resources litigating claims that will not be presented at trial, and it would continue to conceal from Intel the claims that will actually be presented at trial. (Intel’s Br. 15-16.) **Second**, even if Intel is given time to reduce the number of prior art references after MI reduces its claims, MI’s proposal still unreasonably requires Intel to disproportionately reduce the number of prior art references to one-half the number of asserted claims. As explained in Intel’s opening brief, this asymmetric limitation is unworkable because “the number of prior art references and obviousness combinations is driven by the number of claim elements at issue,” which often exceeds the number of claims and therefore requires more than one reference per claim. (*Id.* at 17-18 (quoting *Altera Corp. v. PACT XPP Techs., AG*, 2015 WL 3830982, at *2 (N.D. Cal. June 19, 2015)).)

As explained in Intel’s opening brief (*see* Intel’s Br. 7, 18; Dkt. 116-10, Ex. 10 [2015-08-26 Email from Mr. Coviello to Mr. Saunders]), Intel is willing to reduce the number of prior art references to 35—a reduction that is reasonable and commensurate in scope with the proposed reduction of MI’s claims to 15—within three months of MI’s reduction of the number of asserted claims.

III. CONCLUSION

MI’s opposition brief confirms that the vast majority of currently asserted claims will be dropped before trial. After nearly two full years of litigation, MI should not be permitted to force Intel to continue litigating the at least 93 claims that indisputably will not be presented at trial or to conceal from Intel the claims that will actually be asserted. MI was required to do its due diligence before filing suit—it should be able to identify the claims it intends to assert now. Intel therefore respectfully requests that the Court order MI to reduce the number of claims to 15 across the five asserted patents within fourteen days of the issuance of the Court’s order.

DATED this 5th day of October 2015.

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CERTIFICATE OF COMPLIANCE WITH L.R. 7-2(b)(2)

I certify that this brief complies with the applicable word-count limitation under LR 7-2(b), 26-3(b), 54-1(c), or 54-3(e) because it contains 4,189 words, including headings, footnotes, and quotations, but excluding the caption, table of contents, table of authorities, signature block, and any certificates of counsel.

DATED this 5th day of October, 2015.

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